

REMARKS

The applicant appreciates the examiner's examination of the application and requests reexamination and reconsideration in view of the following remarks.

The examiner rejected claims 1, 3-18, and 20-38 under 35 U.S.C. 102(b) as being anticipated by Ho, U.S. Patent 5,903,469.

With respect to claim 1, claim 1 recites maintaining a circuit design parameter file ... the ... file specifying a physical characteristic of the circuit, monitoring ... to detect the addition of a circuitry component to the circuit ... updating a circuit design parameter file based on ... one design parameter included in the component design parameter file; and providing ... feedback concerning the physical characteristic of the circuit .... At least these features are neither described nor suggested by Ho.

In Ho's method "a user creates a circuit schematic and a layout for an integrated circuit" (Col. 9 line 56-57) and the "geometries of the layout are referenced and interrelated by the nets and circuit elements of the circuit schematic" (Col. 9 line 66- Col. 10, line 5) during the extraction. In contrast, the applicant's method provides feedback on physical characteristics (e.g. layout space, number of gates, number of transistors) based on circuit components (e.g. NAND gates, XOR gates, etc.). Thus, Ho's method neither describes nor suggest claim 1.

Ho further does not suggest "monitoring a design environment to detect the addition of a circuitry component" and providing the user with "feedback concerning the physical characteristic of the circuit."

Ho's method executes extraction in response to a user input. A user can "select a net or nets graphically for extraction... A user may also select a net by entering a schematic net name and layout net number, or schematic block name" (Col. 10, lines 58-61). Ho neither describes nor suggests "monitoring a design environment to detect the addition of a circuitry component to the circuit" as in the applicant's claim 1, thus further differentiating the applicant's method from the method of Ho.

With respect to claims 18, 35 and 37, claim 18 relates to an estimation process, claim 35 relates to a computer program, and claim 37 relates to a processor and memory. Claims 18, 35

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Serial No. : 09/941,519  
Filed : August 29, 2001  
Page : 11 of 11

Attorney's Docket No.: 10559-605001 / P12889

and 37 all include providing feedback concerning a physical characteristic of a circuit based on a circuitry component and/or monitoring a design environment to detect the addition of a circuitry component to the circuit. These limitations are similar to claim 1 and thus, claims 18, 35 and 37 are patentable for at least the same reasons as claim 1.

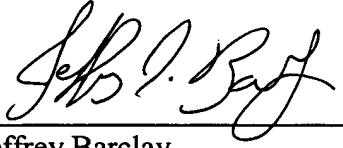
Claims 3-17, 20-35, and 36 are patentable for at least the same reasons as the claims on which they depend.

Applicant asks that all claims be allowed.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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